證據一

【19】中華民國 【12】專利公報 （B）

【11】證書號數： I230992
【45】公告日： 中華民國 94 (2005) 年 04 月 11 日
【51】Int. Cl.[7]： H01L21/60

發明 全 9 頁

【54】名 稱： 半導體裝置
SEMICONDUCTOR DEVICE

【21】申請案號： 093101884 【22】申請日期： 中華民國 93 (2004) 年 01 月 28 日
【11】公開編號： 200425362 【43】公開日期： 中華民國 93 (2004) 年 11 月 16 日
【30】優先權： 2003/01/29 日本 2003-020971

【72】發 明 人：
西田久滋 NISHIDA, HISASHIGE
曾田義樹 SOTA, YOSHIKI
十楚博行 JUSO, HIROYUKI
【71】申請人：
夏普股份有限公司 SHARP KABUSHIKI KAISHA
日本

【74】代理人：林志剛 先生

1

2

[57]申請專利範圍：

1.一種半導體裝置，其特徵為：
將設有外部拉出電極之一個以上的半導體晶片積層於積層基台，
並且，至少具備一個形成連接配線的中介晶片，
並且，設置於至少一個上述半導體晶片之外部拉出電極係藉由引線銲接，連接於至少一個上述中介晶片之上述連接配線，同時，
設置於與上述連接配線連接之上述半導體晶片的外部拉出電極，係中繼該連接配線，而與設置於上述積層基台或其他半導體晶片之配線的電極電性連接。

2.如申請專利範圍第1項所記載之半導體裝置，其中，上述中介晶片係使用與形成上述半導體晶片時所使用之晶圓相同材質及構造的晶圓而形成者。

3.如申請專利範圍第1項所記載之半導

3

體裝置，其中，上述中介晶片係利用與形成上述半導體晶片相同的裝置而形成者。

4.如申請專利範圍第1項所記載之半導體裝置，其中，上述半導體晶片除了外部拉出電極以外的部分係由表面保護膜覆蓋。

5.如申請專利範圍第1項所記載之半導體裝置，其中，在上述插入晶片的積層上方，至少積層一個半導體晶片。

6.如申請專利範圍第5項所記載之半導體裝置，其中，在設置於上述中介晶片的連接配線上設有：
第1銲墊，其係藉由引線銲接，與設置於上述中介晶片之積層下方的外部電極電性連接，和
第2銲墊，其係藉由引線銲接，與設置於上述中介晶片之積層上方的外部電極電性連接。

7.如申請專利範圍第1項所記載之半導體裝置，其中，上述中介晶片和上述半導體晶片係並列設置於上述積層基台或其他半導體晶片上。

8.如申請專利範圍第7項所記載之半導體裝置，其中，在設置於上述中介晶片的連接配線上設有：
第1銲墊，其係藉由引線銲接，與設置於上述中介晶片之積層下方的外部電極電性連接，和
第2銲墊，其係藉由引線銲接，與和上述中介晶片並列設置之半導體晶片的電極電性連接。

9.如申請專利範圍第6或8項所記載之半導體裝置，其中，於上述中介晶片上設有複數連接配線，同時，上述複數連接配線是以彼此不會交叉之方式配置。

10.如申請專利範圍第9項所記載之半導體裝置，其中，第1銲墊的排列順序、和藉由上述連接配線與該第1銲墊連接之第2銲墊的排列順序不同。

11.如申請專利範圍第6或8項所記載之半導體裝置，其中，在上述中介晶片上設有複數連接配線，同時，上述複數連接配線係引線地配置。

12.如申請專利範圍第6或8項所記載之半導體裝置，其中，在上述中介晶片的連接配線上，於上述第1銲墊和上述第2銲墊之間，設置至少一個其他銲墊，同時，
於上述第1銲墊、和上述第2銲墊、和上述其他銲墊中，使用任意兩個銲墊，與外部電極進行引線銲接。

13.如申請專利範圍第12項所記載之半導體裝置，其中，於上述中介晶片上設有複數連接配線，同時，上述複數連接配線是以彼此不會交叉之方式配置。

14.如申請專利範圍第13項所記載之半導體裝置，其中，於上述第1銲墊的排列順序、和藉由上述連接配線與該第1銲墊連接之上述第2銲墊的排列順序、和藉由上述連接配線與該第2銲墊連接之上述其他銲墊的排列順序中，至少兩個銲墊的排列順序不同。

圖式簡單說明：

第1圖(a)是表示本發明第1實施型態之半導體裝置構成的俯視圖。

第1圖(b)是第1圖(a)之A－A'箭號的剖視圖。

第2圖(a)是表示本發明第2實施型態之半導體裝置構成的俯視圖。

第2圖(b)是第2圖(a)之B－B'箭號的剖視圖。

第3圖(a)是表示本發明第3實施型態之半導體裝置構成的俯視圖。

第3圖(b)是第3圖(a)之C－C'箭號的剖視圖。

5

第4圖是表示本發明第4實施型態之半導體裝置具有中介晶片之構成的俯視圖。

第5圖(a)是表示在第4圖所示之中介晶片上，積層半導體晶片之半導體裝置的俯視圖。

第5圖(b)是第5圖(a)之D－D'箭號的剖視圖。

第6圖是表示本發明第5實施型態之半導體裝置具有中介晶片之構成的俯視圖。

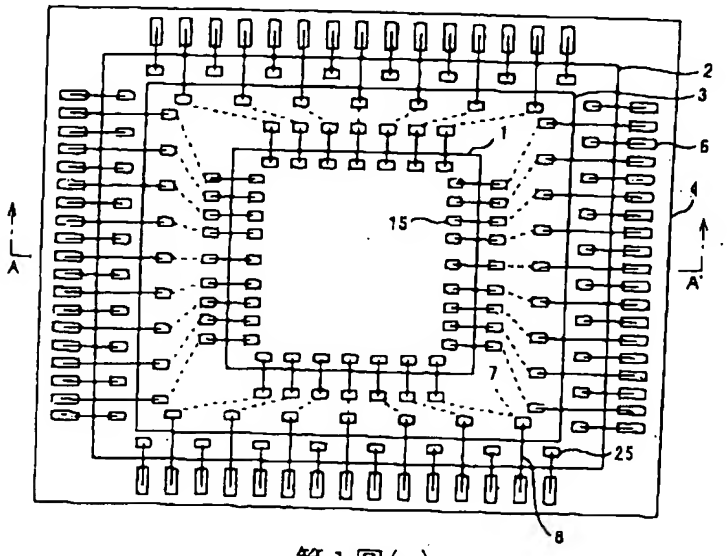
6

第7圖是表示在第6圖所示之中介晶片上，積層半導體晶片之半導體裝置的俯視圖。

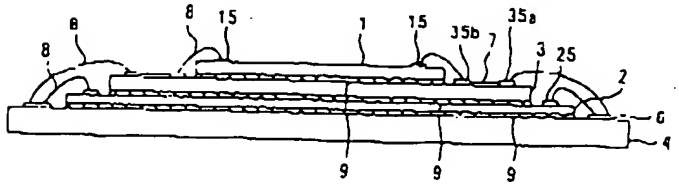
第8圖是表示在第6圖所示之中介晶片上，積層與第7圖不同的半導體晶片之半導體裝置的俯視圖。

第9圖(a)是表示習知半導體裝置之構成例的俯視圖。

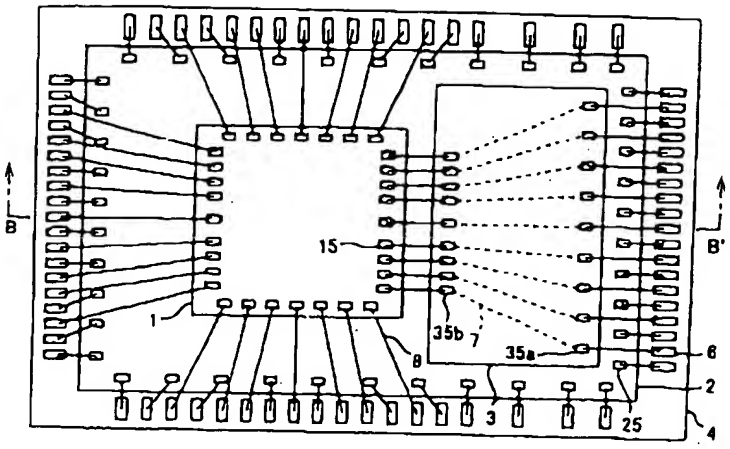
第9圖(b)是第9圖(a)之E－E'箭號的剖視圖。



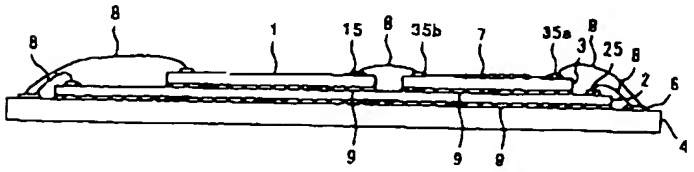
第1圖(a)



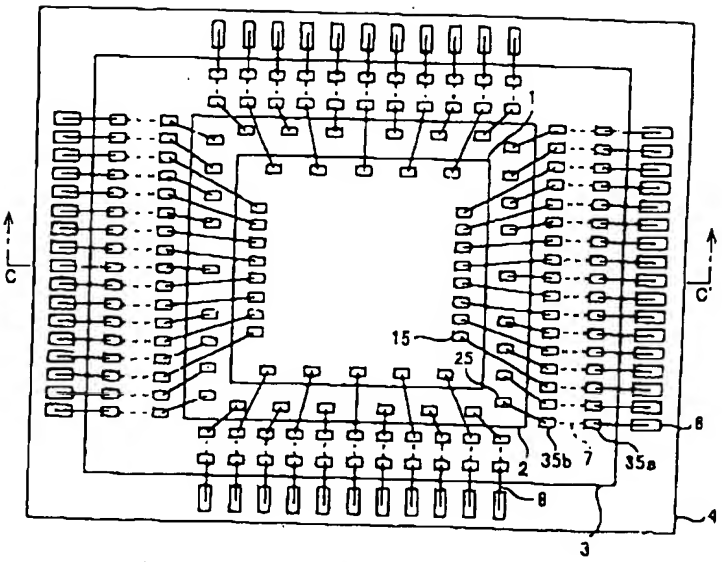
第1圖(b)



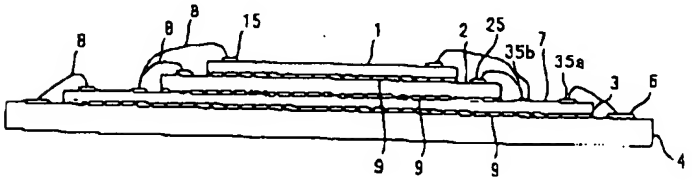
第2圖(a)



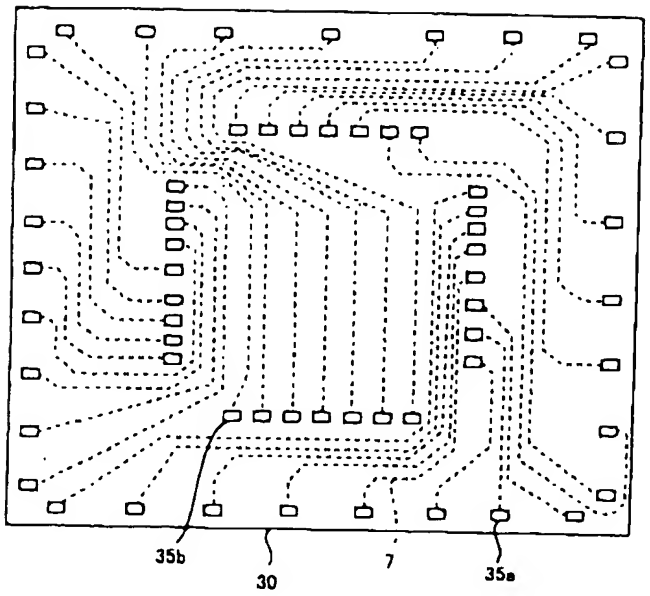
第2圖(b)



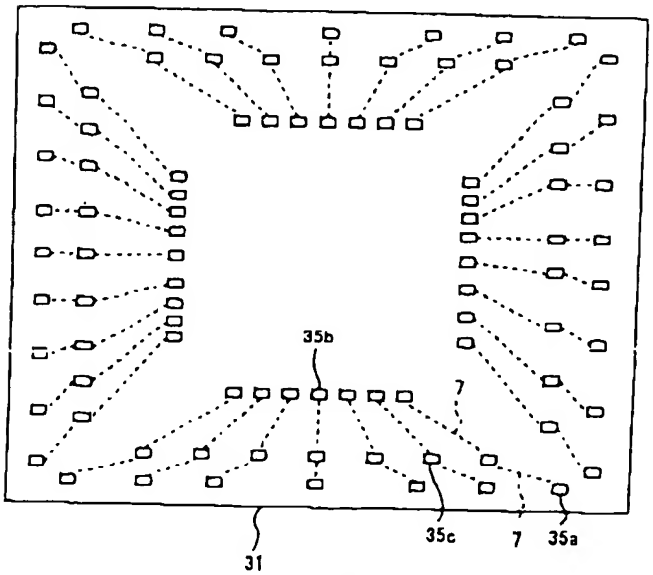
第3圖(a)



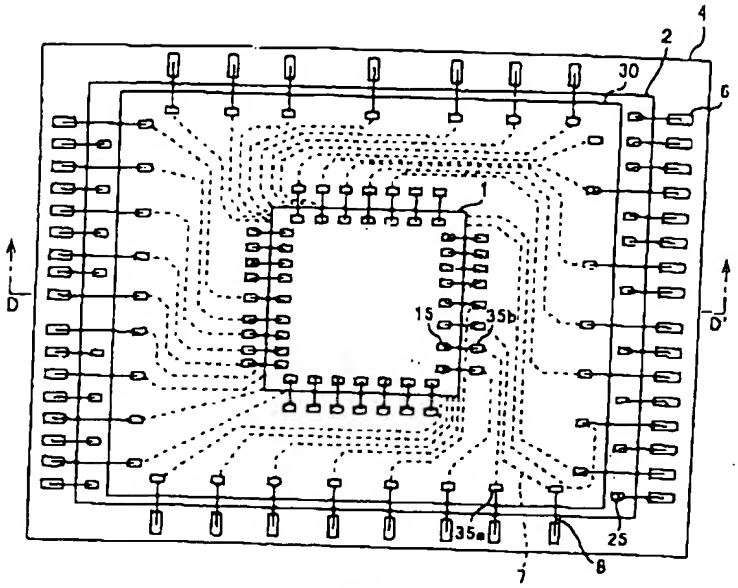
第3圖(b)



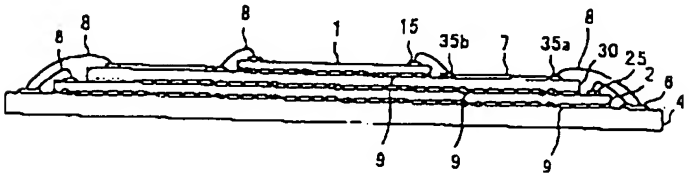
第 4 圖



第 6 圖

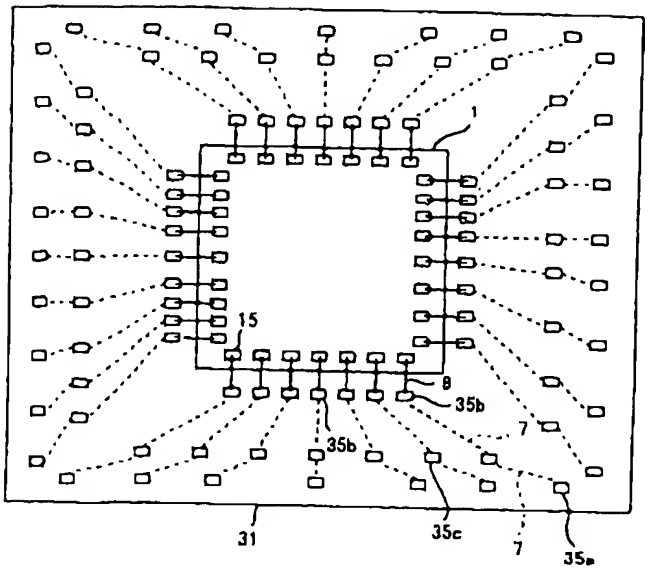


第5圖(a)

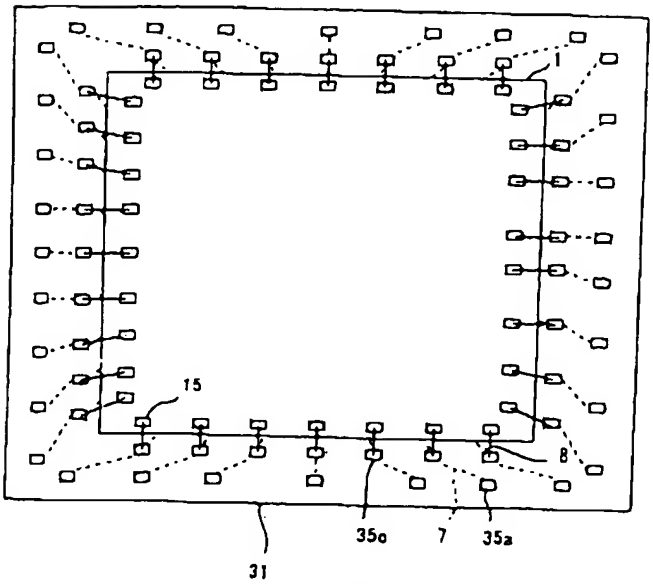


第5圖(b)

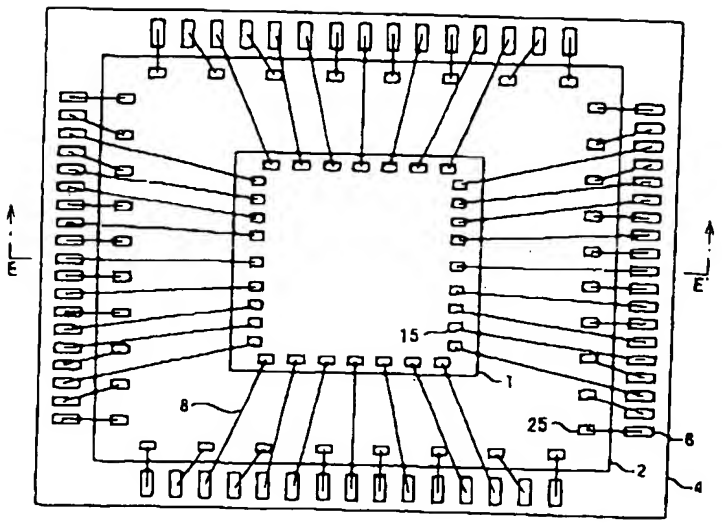
(8)



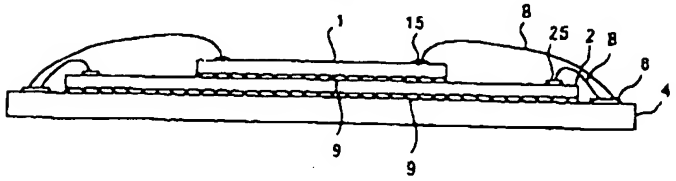
第 7 圖



第 8 圖



第 9 圖(a)



第 9 圖(b)

Taiwanese Unexamined Utility Model Publication No. 562240

[TITLE OF THE INVENTION] ELECTRONIC PACKAGE INCLUDING WIRE BONDING CHIP

[ABSTRACT]

An electronic package includes a substrate (21), a function chip (22) attached to the substrate by soldering, a wire bonding chip (23) attached to the substrate by soldering and which is positioned on one side of the function chip, a resin encapsulation body (25) attached to the substrate for protecting the function chip and the wire bonding chip (23), plural gold wires (24), and plural electric connection terminals (26) attached on a bottom surface of the substrate by soldering. One of the plural gold wires electrically connects a predetermined bump (223) of the function chip to a corresponding bonding pad (3) of the wire bonding chip (23). Moreover, another gold wire electrically connects the bonding pad (3) to an electric connection pad (214) on the substrate *(24(sic))*. The electric connection pad (214) is to be electrically connected to a bump of the function chip. This makes it possible to transmit an electric signal processed by the function chip to the circuit substrate. This results in a reduction in a length of the gold wire and an angle of gradient of the gold wire. Accordingly, a package yield is improved.

[TECHNICAL FIELD]

The present utility model relates to an electronic package.

Especially, the utility model relates to an electronic package including plural chips.

[BACKGROUND]

In order to realize reduction in size, weight, and thickness in an electronic product, instead of only one function being provided to a single electronic package, plural different functions are provided to an electronic package by sealing in the electronic package a chip module including plural different functions. This leads to reduction in a number of electronic parts mounted on a circuit substrate of the electronic product. Reducing a volume of an electronic product by the reducing a number of electronic parts in this manner is a concept that has been already studied for a long time in this industry. Different technical features are respectively disclosed in, for example, Taiwanese Patent No. 428258 "SEMICONDUCTOR DEVICE INCLUDING CONNECTING TERMINAL IN GRID ARRAY SYSTEM", Taiwanese Patent No. 443582 "STRUCTURE OF MULTI-CHIP PACKAGE", Taiwanese Patent No. 484749 "MULTI-CHIP PACKAGE TECHNIQUE APPLIED TO BALL GRID ARRAY PACKAGE PROCESS", Taiwanese Patent No. 498513 "MULTI-CHIP WIRING PACKAGE OF MICRO MACHINE", USP 0153615A1/2002 "MULTI-CHIP PACKAGE TYPE SEMICONDUCTOR DEVICE", USP 6407456B1 "MULTI-CHIP DEVICE UTILIZING A FLIP CHIP AND WIRE BOND ASSEMBLY", and the like.

As illustrated in FIGS. 1 and 2, in general, an electronic package 1 including a plural number of chips having different

functions includes a substrate 11, a plural function chips 12 and 12' stacked in order from an upper side of the substrate 11 (In this embodiment, an example, in which two function chips are used, is explained.), plural gold wires 13 electrically connecting (i) the substrate 11 to the function chips 12 and 12' and (ii) the function chip 12 to the function chip 12', a resin encapsulation body 14 attached to the substrate 11 and covering these function chips 12 and 12' and the metal wires 13, and plural electric connection terminals 15 attached to a bottom surface of the substrate 11 by soldering.

As a person skilled in a wire bonding process (wire bond) of an encapsulation process knows, there are differences in heights respectively (i) between the substrate 11 and the function chip 12, (ii) between the function chip 12 and the function chip 12', and (iii) between the substrate 12*(sic)* and the function chip 12' constituting a top layer. Therefore, when the substrate 11 and the function chips 12 and 12' are connected electrically by the gold wires 13, the wire bonding process becomes difficult due to the differences in the heights. As a result, a yield is deteriorated and a molding flow in a subsequent resin packaging process becomes too complex to control. This makes the resin packaging process more difficult.

Moreover, in a case where (i) a difference between areas of the two function chips 12 and 12' is large to an extreme and/or (ii) a difference between areas of the function chip 12' and the substrate 11 is large to an extreme, lengths of the gold wires 13 increases. As

a result, each gold wire 13 which has increased in length sits loosely and undulates. The gold wire 13 becomes likely to contact adjacent gold wires 13 and produces a short circuit. Further, an angle between the wire 13 and one side of the function chips 12 and 12' becomes too small. This does not agree with a design rule determined by a client. This leads to an increase in cost that a producer needs to bear.

Moreover, a packaging method in which the function chips 12 and 12' are stacked in order, in this manner, naturally increases a thickness of the electronic package 1. In order to maintain a standard thickness of a standard electronic package, a complex problem in the process of, for example, how to reduce (i) a thickness of the function chips 12 and 12' and the substrate 11, (ii) the length of the gold wire 13, and the like needs to be solved.

As mentioned above, sealing plural function chips 12 and 12' in the electronic package 1 by the method, in which the function chips 12 and 12' are stacked, makes it possible to reduce a number of electronic packages in an electronic product undoubtedly. This results in attaining the object to reduce a volume of the electronic product. However, in such a packaging method, other than the problems in (i) the increase in the thickness of the electronic package 1 and (ii) the disagreement with the standard, it is necessary to study and improve the wire bonding process in order to improve the reliability of gold wires.

[DISCLOSURE OF THE UTILITY MODEL]

Therefore, an object of the present utility model is to provide an electronic package having a wire bonding chip with improved reliability, the wire bonding chip having a reduced gold wire length and a reduced angle between a gold wire and a chip.

According to the present utility model, an electronic package having a wire bonding chip, includes (i) a substrate (21) which includes a predetermined circuit layout (213) and plural electric connection pads (214) electrically connected to the circuit layout, (ii) a function chip (22), attached onto the substrate by soldering, which is capable of processing an electric signal and which also includes plural bumps (223) electrically connected to the electric connection pads (214) of the substrate respectively, the plural bumps (223) corresponding to electric connection pads (214), (iii) a resin encapsulation body (25), attached to the substrate, which resin encapsulation body covers the circuit layout (213) of the substrate, the plural electric connection pads (214), and the function chip (22) so as to block the outside air, and (iv) plural electric connection terminals (26), provided on an opposite side of a substrate surface to which a bottom surface of the function chip is attached by soldering, which electric connection terminals (26) are electrically connected to the circuit layout of the substrate, and which are, further, electrically connected to a circuit substrate, the electronic package further includes: at least a wire bonding chip (23), attached onto the substrate by soldering, which includes plural bonding pads (3) that do not conduct electricity between each other,

each of the plural bonding pads (3) including a first soldering section (31) and a second soldering section (32) which are apart from each other but conduct electricity between each other; and plural gold wires (24), wherein: the first soldering section (31) is positioned close to a predetermined bump (223) of the function chip (22); the second soldering section (32) is positioned close to one electric connection pad (214) out of the electric connection pads (214) of the substrate (21), which electric connection pad (214) a predetermined bump of the function chip is connected to; one of the gold wires electrically connects the predetermined bump (223) of the function chip (22) to the first soldering section (31) of the bonding pad; another one of the gold wires electrically connects the second soldering section (32) to the predetermined electric connection pad (214) of the substrate (21); and electrical connections made by the gold wires allow an electric signal processed by the function chip to be transmitted to the circuit substrate.

[EMBODIMENT OF THE UTILITY MODEL]

The above and other technical contents, features, and advantages of the present utility model will be evident from exemplary embodiments explained in detail with reference to the drawings. In the description below, like elements are denoted with the like reference numbers.

As illustrated in FIGS.3 and 4, in a first embodiment of an electronic package 2 including a wire bonding chip of the present utility model, a substrate 21, a function chip 22 attached to the

substrate 21 by soldering, a wire bonding chip 23 attached to the substrate 21 by soldering, plural gold wires 24, a resin encapsulation body 25 attached to the substrate 21, and plural electric connection terminals 26 are included.

The substrate 21 has a rectangular shape. The substrate 21 includes an upper surface 211, a bottom surface 212 on an opposite side of the upper surface 211, a circuit layout 213 having a predetermined pattern, and plural electric connection pads 214 and 214'. A design pattern of the circuit layout 213 differs according to a predetermined electric function of the function chip 22. Because this part is not a concern of the present utility model, the detailed explanation thereof is omitted. The electric connection pads 214 and 214' are positioned on fringe sections of the upper surface 211 and the bottom surface 212 respectively. The pads 214 and 214' are also electrically connected to the circuit layout 213.

The function chip 22 can receive a calculation signal, a transmission signal, and an electric signal. The function chip 22 includes a bottom surface 221 attached to the upper surface 211 of the substrate 21, an electric connection surface 222 on an opposite side of the bottom surface 221, and plural bumps 223 provided on the electric connection surface 222. These bumps 223 are respectively electrically connected to electric connection pads 214 provided on the upper surface 211 of the substrate 21 by plural gold wires 24 predeterminedly corresponding to the respective bumps 223.

The wire bonding chip 23 does not include any electronic calculating function. However, a production process of the wire bonding chip 23 adopts a semiconductor manufacturing process used for the function chip 22. By making the wire bonding chip 23 out of silicon and/or a compound including silicon, a thickness of the wire bonding chip 23 corresponds to a thickness of the function chip 22. The wire bonding chip 23 also includes a bottom surface 231 attached to the upper surface 211 of the substrate 21, a surface 232 for gold wires on an opposite side of the bottom surface 231, and plural bonding pads 3 which do not conduct electricity between each other (which do not intersect each other).

Each of the bonding pads 3 is made of a conductive material, for example, gold, nickel, copper, aluminum, or an alloy including a component such as gold, nickel, copper, aluminum, and the like. The bonding pads 3 are provided on the surface 232 of the wire bonding chip 23 in a predetermined manner. In selecting materials as mentioned above, a material for the gold wires needs to be selected appropriately. Bonding the gold wires 24 and the bonding pads 23 when both are made of the same or similar materials provides the strongest bonding between the gold wires 24 and the bonding pads 23.

The bonding pads 3 mentioned above are provided apart from each other, and each of the bonding pads 3 includes a first soldering section 31 and a second soldering section 32 which do not conduct electricity between each other. The first soldering sections

31 are close to predetermined bumps 223 of the function chip 22. The second soldering sections 32 are close to the electric connection pads 214 of the substrate 21. In this embodiment, these bonding pads 3 are respectively formed so as to have an L-shape or a rectangular shape. Sequentially, the first soldering sections 31 are provided in a concentrated manner and the second soldering sections 32 are distributed in a radial pattern in a widely spreading manner. This causes the first soldering sections 31 to be relatively closer to the bumps 223 of the chip 22 and the second soldering sections 32 to be relatively closer to the electric connection pads 214 of the substrate 21. Here, distribution patterns of bumps of function chips and electric connection pads of substrates, which function chips and substrates are applied especially to different electronic products, differ from one another. Accordingly, a shape of a wire bonding chip needs to be adjusted for different function chips and substrates. At the same time, the shape and a distribution pattern of plural bonding pads of the wire bonding chip also need to be adjusted to a distribution pattern of bumps of the function chip and electric connection pads of the substrate. These configuration patterns vary in many ways. Therefore, the explanation of each pattern is omitted here.

As a person skilled in an encapsulation technique knows, a predetermined bump 223 of the function chip 22 is electrically connected to a predetermined electric connection pad 214 of the substrate 21 by one gold wire 24 only, in a conventional art. In this

manner, an object of connecting the function chip 22 and the substrate 21 electrically is attaincd. However, in this utility model, first, a predetermined bump 223 of the function chip 22 among plural bumps 223 close to the wire bonding chip 23 is electrically connected to the first soldering section 31 of the bonding pad 3 by one of the gold wires 24. Then, the second soldering section 32 and a predetermined electric connection pad 214 of the substrate 21 are electrically connected by another one of the gold wires 24. The bumps 223 of the function chip 22 on sides different to that of the predetermined bump are electrically connected to the electric connection pads 214 of the substrate 21 by a general wire bonding method. This improves a yield in a wire bonding process as well as being able to reduce a length and a height of original gold wires 24. By electrically connecting the bumps of the function chip 22 to the plural electric connection pads 214 of the substrate 21 in order by these gold wires 24 in this manner, transmission of an electric signal calculated by the function chip 22 to the substrate 21 becomes possible.

The resin encapsulation body 25 is a polymer. The resin encapsulation body 25 is attached to the upper surface 211 of the substrate 21. The resin encapsulation body 25 blocks out the outside air by covering the plural electric connection pads 214 of the circuit layout 213, the upper surface 211 of the substrate 21, the function chip 22, the wire bonding chip 23, and the plural gold wires 24 so as to prevent oxidation and corrosion.

The electric connection terminals 26 are respectively attached to the corresponding plural electric connection pads 214' of the bottom surface 212 of the substrate 21 by soldering, and electrically connected to the circuit layout 213 of the substrate 21. The electric connection terminals 26 cause the electronic package 2 to be electrically connected to a circuit substrate (not illustrated) of a predetermined electronic product. The electric connection terminals 26 causes an electric signal calculated by the function chip 22 to be transmitted to the substrate 21 and then further to the circuit substrate, and makes the electronic package 2 perform a predetermined function.

As mentioned above, in the present utility model, a wire bonding chip 23, which does not include an electronic calculating function, is provided on one side of the function chip 22 by soldering. The bumps 223 of the function chip 22 and the electric connection pads 214 of the substrate 21, which are originally intended to be connected electrically, are connected via the plural bonding pads 3, which do not conduct electricity between each other, by (i) first electrically connecting the bumps 223 of the function chip 22 and the bonding pads 3 respectively by two gold wires 24 *(sic)* and (ii) further electrically connecting the bonding pad 3 and the electric connection pad 214 of the substrate 21 by another gold wire 224*(sic)*. This makes it possible to drastically reduce the length of the gold wire 24 and the height of the gold wire 24. Accordingly, as a person skilled in a semiconductor process and

an encapsulation technique knows, although material cost increases partially due to an addition of the one wire bonding chip 23, the cost can be reduced in total. At the same time, because the reduction in length and height of the original gold wire 24 is possible, a degree of control of the gold wire 24 and a yield in the wire bonding process can be improved. Furthermore, because the shorter and lower gold wire 24 does not affect a molding flow in a subsequent resin packaging process, a yield in the packaging process can be improved. As a result, the present utility model can respond to a need of producers by reducing total production cost.

In the present utility model, a difference in areas of the function chip 22 and the substrate 21 is within a predetermined range. By changing relative positions of the function chip 22 and the substrate 21 and, moreover, by providing the wire bonding chip 23, all the parameters of the gold wire, for example, height of the gold wire 24, the length of the gold wire 24, an angle between the gold wire 24 and one side of the function chip 22, and the like, can be arranged to meet a design rule required by a client.

Because the difference in areas of the function chip 22 and the substrate 21 is extremely large, all the parameters of the gold wire, for example, height of the gold wire 24, the length of the gold wire 24, an angle between the gold wire 24 and one side of the function chip 22, and the like may not be able to meet a design rule required by a client even if relative positions of the function chip 22 and the substrate 21 are changed and, moreover, the wire bonding

chip 23 is provided. In such a case, as illustrated in FIG.5, namely, as described in a second embodiment including an electronic package 2' including the wire bonding chip of the present utility model, plural different wire bonding chips 23 and 23' are provided on different sides of the function chip 22. In this embodiment, an example in which two wire bonding chips 23 and 23' are provided on two sides adjacent to the function chip 22 is explained. This shortens and reduces the original length and height of the gold wire 24. A detailed structure of the example has already been explained in the first embodiment. Accordingly, the explanation is omitted here.

FIG.6 is a third embodiment of an electronic package having the wire bonding chip of the present utility model. This embodiment is similar to the two embodiments mentioned above. However, this embodiment is different from other embodiments in that, when a different function chip 22 is designed, according to a demand for a circuit, plural gold wires 24 connected to the pad 223 *(sic)* of the function chip 2 *(sic)* often need to be connected to corresponding plural electric connection pads 214 of the substrate 21 by soldering, or plural gold wires 24 connected to the plural bumps 223 of the function chip 22 often needs to be connected to a corresponding electric connection pad 214 of the substrate 21 by soldering. Accordingly, in the present embodiment, all of the first soldering section 31 and the second soldering section 32 of bonding pads 3 of an electronic package 2" are connected to at least one end of one of

the gold wires 24 selectively by soldering. The materials of the bonding pads 3 and the gold wires 24 are same or similar. Therefore, even when plural gold wires 24 are connected to the first and the second soldering sections 31 and 32, by soldering, the first and the second soldering sections 31 and 32 do not affect a connection section of each of the gold wires 24. Accordingly, the present utility model is applied to an electrical connection of the different function chip 22.

Moreover, the electronic package having the wire bonding chip of the present utility model is also applied to the conventional electronic package in which plural function chips are stacked. In this case, only one or plural layer(s) of a function chip(s) needs to be added between (i) the wire bonding chip 23 and the function chip 22 and (ii) the substrate 21. There are many variations to which such a structure is applied. The explanation thereof is omitted.

Overall, the present utility model relates to the electronic packages 2 and 2' respectively including the wire bonding chips. By providing the wire bonding chips 23 and 23' that do not include an electronic calculating function, the length of a gold wire 24 and the height of the gold wire 24 are reduced. At the same time, a degree of a control of the wire bonding can be improved. Moreover, a yield of the packaging process can be improved because an influence to the molding flow of the subsequent resin packaging process is reduced. Therefore, the total production cost can be reduced. As a result, the present utility model can respond to needs of producers, and

accordingly, the object of the present utility model can be attained reliably.

The present utility model is not limited to the description of the embodiments mentioned above, but may be altered in various ways within the scope of the claims.

[BRIEF DESCRIPTION OF DRAWINGS]

FIG.1 is a cross-sectional view of a structure of a BGA (Ball Grid Array) package including chips stacked in plural layers according to the conventional art.

FIG.2 is a plan view of FIG.1, which plan view illustrates a pattern in which the chips stacked in the plural layers are electrically connected by gold wires.

FIG.3 is a cross-sectional view illustrating a structure of a first embodiment of an electronic package having a wire bonding chip of the present utility model.

FIG.4 is a plan view of FIG.3, which plan view illustrates a pattern in which a function chip, the wire bonding chip, and a substrate are electrically connected each other by gold wires.

FIG.5 is a plan view of a second embodiment of an electronic package including wire bonding chips, which plan view illustrates a pattern in which lengths and distribution angles of gold wires are reduced by electrically connecting the function chip to the substrate via the two wire bonding chips by gold wires.

FIG.6 is a plan view of a third embodiment of an electronic package having a wire bonding chip of the present utility model,

which plan view illustrates that each of the first soldering section and the second soldering section included in each of the bonding pads is connected to at least one end of one of the gold wires selectively by soldering.

[EXPLANATION OF REFERENCE NUMERALS]

1: Electronic package

11: Substrate

12, 12': Function Chip

13: Gold Wire(s)

14: Resin Encapsulation Body

15: Electric Connection Terminal

2, 2', 2": Electronic package

21: Substrate

211: Upper Surface

212: Bottom Surface

213: Circuit Layout

214, 214': Electric Connection Pad

22: Function Chip

221: Bottom Surface

222: Electric Connection Surface

223: Bump

23, 23': Wire Bonding Chip

231: Bottom Surface

232: Surface For Gold Wires

24: Gold Wire(s)

25: Resin Encapsulation Body

26: Electric Connection Terminal (Ball)

3: Bonding Pad

31: First Soldering Section

32: Second Soldering Section

[CLAIMS]

1. An electronic package having a wire bonding chip, comprising (i) a substrate (21) which includes a predetermined circuit layout (213) and plural electric connection pads (214) electrically connected to the circuit layout, (ii) a function chip (22), attached onto the substrate by soldering, which is capable of processing an electric signal and which also includes plural bumps (223) electrically connected to the electric connection pads (214) of the substrate respectively, the plural bumps (223) corresponding to electric connection pads (214), (iii) a resin encapsulation body (25), attached to the substrate, which resin encapsulation body covers the circuit layout (213) of the substrate, the plural electric connection pads (214), and the function chip (22) so as to block the outside air, and (iv) plural electric connection terminals (26), provided on an opposite side of a substrate surface to which a bottom surface of the function chip is attached by soldering, which electric connection terminals (26) are electrically connected to the circuit layout of the substrate, and which are, further, electrically connected to a circuit substrate, the electronic package further comprising:

at least a wire bonding chip (23), attached onto the substrate by soldering, which includes plural bonding pads (3) that do not conduct electricity between each other, each of the plural bonding pads (3) including a first soldering section (31) and a second soldering section (32) which are apart from each other but conduct electricity between each other; and

plural gold wires (24), wherein:

the first soldering section (31) is positioned close to a predetermined bump (223) of the function chip (22);

the second soldering section (32) is positioned close to one electric connection pad (214) out of the electric connection pads (214) of the substrate (21), which electric connection pad (214) a predetermined bump of the function chip is connected to;

one of the gold wires electrically connects the predetermined bump (223) of the function chip (22) to the first soldering section (31) of the bonding pad;

another one of the gold wires electrically connects the second soldering section (32) to the predetermined electric connection pad (214) of the substrate (21); and

electrical connections made by the gold wires allow an electric signal processed by the function chip to be transmitted to the circuit substrate.

2. The electronic package having the wire bonding chip as set forth in Claim 1, wherein:

a thickness of the wire bonding chip corresponds to a thickness of the function chip.

3. The electronic package having the wire bonding chip as set forth in Claim 1, wherein:

the wire bonding chip is made of silicon or a compound including silicon.

4. The electronic package having the wire bonding chip as set forth in Claim 1, wherein:

the bonding pads of the wire bonding chip are made of a conductive material.

5. The electronic package having the wire bonding chip as set forth in Claim 4, wherein:

the bonding pads of the wire bonding chip are made of gold, nickel, copper, aluminum, an alloy including at least gold, an alloy including at least nickel, an alloy including at least copper, and/or an alloy including at least aluminum.

6. The electronic package having the wire bonding chip as set forth in Claim 1 wherein:

the bonding pads of the wire bonding chip are applied on one surface of the wire bonding chip in a predetermined manner.

7. The electronic package having the wire bonding chip as set forth in Claim 1 wherein:

each of the first soldering section and the second soldering section included in each of the bonding pads is connected to at least one end of one of the gold wires selectively by soldering.

證據二

中華民國專利公報 [19] [12]

[11]公告編號：562240
[44]中華民國 92年 (2003) 11月11日
新型 全 5 頁

[51] Int.Cl.[7] ： H01L23/043

[54]名 稱：具有打線橋接晶片之電子封裝件

[21]申請案號： 092201476 [22]申請日期：中華民國 92年 (2003) 01月27日

[72]創 作 人：
劉文俊 屏東縣屏東市信和里泰和五號
劉仲杰 高雄市前鎮區英明一路九十七之一號
洪慧齡 高雄市鼓山區鼓山二路二〇二巷四號
[71]申 請 人：
華東科技股份有限公司 高雄市高雄加工出口區北一路十八號
[74]代 理 人： 惲軼群 先生
陳文郎 先生

1 2

[57]申請專利範圍：

1.一種具有打線橋接晶片之電子封裝件，該電子封裝件包含一基板、一銲黏於該基板上之功能晶片、一與該基板相連結之封裝膠體，及多數銲黏於該基板相反於銲黏該功能晶片之一底面上的電性連接件，該基板具有預定電路佈局及多數分別與該電路佈局相電性連結之電性連接墊，該功能晶另可處理電子信號，並具有多數分別與該基板之電性連接墊預定相對應電性連結之電子節墊，該封裝膠體包覆該基板之電路佈局、多數電性連接墊與該功能晶片而與外界相隔絕，該些電性連接件與該基板之電路佈局相電性連結，並可電性連結至一電路機板上；其特徵在於：

該電子封裝件更包含至少一銲黏於該基板上之打線橋接晶片，及多數銲線，該打線橋接晶片包括多數彼此不相電性導通之架橋銲墊，該每一架橋銲墊具有二相對遠離並相互電性導通之第一銲黏部與第二銲黏部，且該第一銲黏部是相對靠近該功能晶片之一預定電子節墊，該第二銲黏部是相對靠近該功能晶片之預定電子節墊預定電性連接之該基板的電性連接墊，同時，以該等銲線其中之一電性連結該功能晶片之預定電子節墊與該架橋銲墊之第一

銲點部，以另一銲線電性連結該第二銲點部與該基板之預定電性連接墊，而使該功能晶片處理之電子信號可傳輸至該電路機板。

2.依據申請專利範圍第1項所述之具有打線橋接晶片之電子封裝件，其中，該打線橋接晶片之厚度是相對應於該功能晶片之厚度。

3.依據申請專利範圍第1項所述之具有打線橋接晶片之電子封裝件，其中，該打線橋接晶片是以矽，及/或包含矽之化合物為材料。

4.依據申請專利範圍第1項所述之具有打線橋接晶片之電子封裝件，其中，該打線橋接晶片之架橋銲墊是以導電材料製成。

5.依據申請專利範圍第4項所述之具有打線橋接晶片之電子封裝件，其中，該打線橋接晶片之架橋銲墊是以金、銀、銅、鋁、至少含金之合金、至少含鎳之合金、至少含銅之合金，及/或至少含鋁之合金製成。

6.依據申請專利範圍第1項所述之具有打線橋接晶片之電子封裝件，其中，該打線橋接晶片之架橋銲墊是以預定態樣鍍佈於該打線橋接晶片之一表面。

7.依據申請專利範圍第1項所述之具有打線橋接晶片之電子封裝件，其中，該每一架橋銲墊之第一銲點部與第二銲點部，是分別可選擇地供至少一條銲線的一端部相銲點。

圖式簡單說明：

第一圖是一剖視圖，說明習知具有複數層相互堆疊之晶片的球格陣列封裝件之結構；

第二圖是第一圖之一正面上視圖，說明該些複數層相互堆疊之晶片以銲線相互電性連結之態樣；

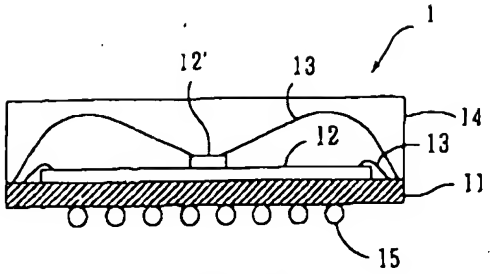
第三圖是一剖視圖，說明本新型具有打線橋接晶片之電子封裝件的一第一較佳實施例之結構；

第四圖是第三圖之一正面上視圖，說明一功能晶片、一打線橋接晶片，及一基板以銲線相互電性連結之態樣；

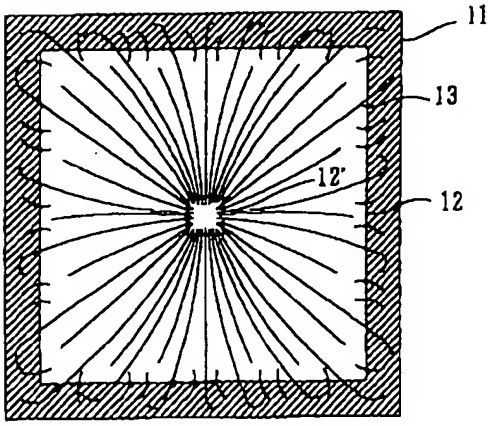
第五圖是本新型具有打線橋接晶片之電子封裝件的一第二較佳實施例之一正面上視圖，並說明一功能晶片藉由二打線橋接晶片而與基板相互以銲線電性連結，以縮短銲線之長度與分布角度之態樣；及

第六圖是本新型具有打線橋接晶片之電子封裝件的一第三較佳實施例之一正面上視圖，並說明一打線橋接晶片之架橋銲墊的第一銲點部與第二銲點部，分別可選擇地供至少一條銲線的一端部相銲點。

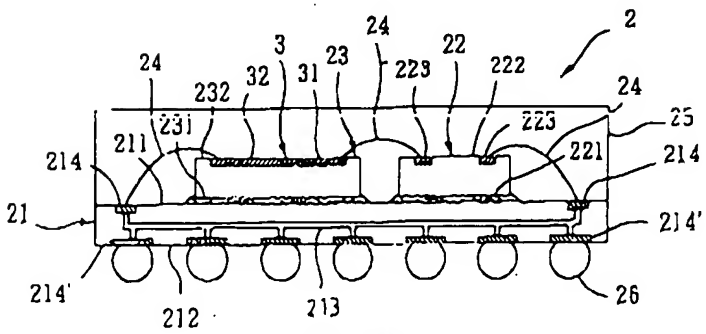
(3)


1
12'
13
14
12
13
11
15

第一圖

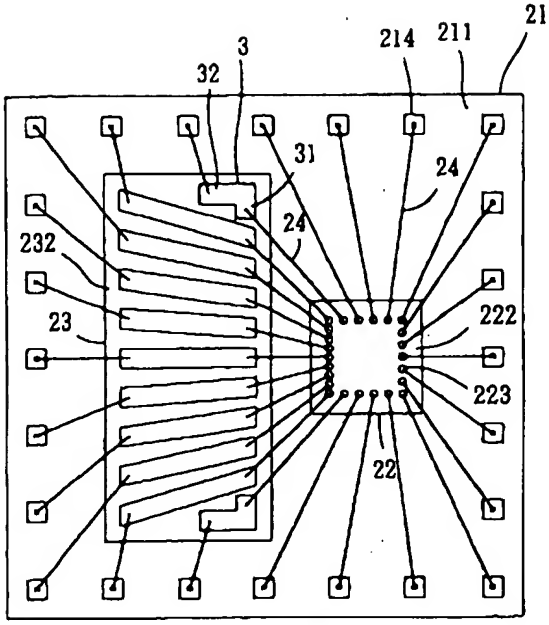

11
13
12'
12

第二圖

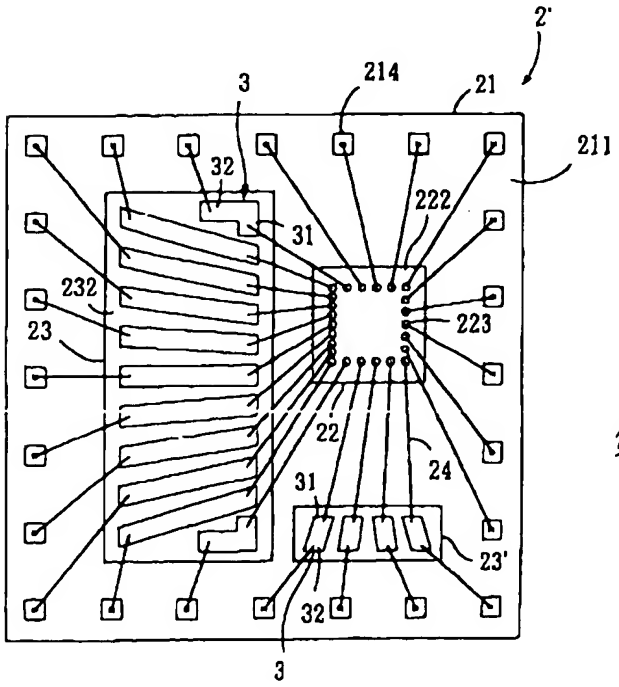

2
24
3
24
22
24
232
32
31
23
223
222
231
223
25
211
221
214
214
214
21
214'
214'
212
213
26

第三圖

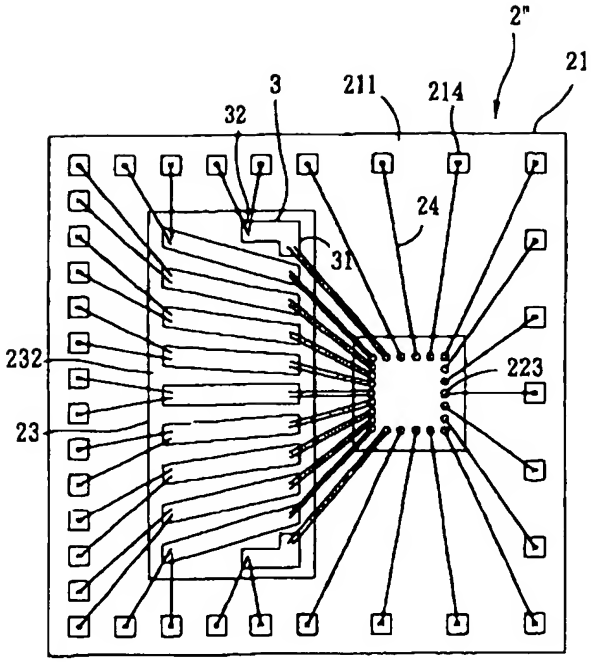
(4)


21
214
211
3
32
31
24
24
232
23
222
223
22

第四圖


2'
3
214
21
211
32
222
31
232
223
23
22
24
31
23'
32
3

第五圖



第六圖

公告本

新型專利說明書 562240

（填寫本書件時請先行詳閱申請書後之申請須知，作※記號部分請勿填寫）

※ 申請案號：092201476 ※IPC分類：H01L 23/03

※ 申請日期：92-01-27

壹、新型名稱

（中文）具有打線橋接晶片之電子封裝件

（英文）

貳、創作人（共 3 人）

創作人 1 （如創作人超過一人，請填說明書創作人續頁）

姓名：（中文）劉文俊

（英文）

住居所地址：（中文）屏東市900信和里榮和5號

（英文）

國籍：（中文）中華民國 （英文）

參、申請人（共 1 人）

申請人 1 （如申請人超過一人，請填說明書申請人續頁）

姓名或名稱：（中文）華東科技股份有限公司

（英文）

住居所或營業所地址：（中文）高雄市806高雄加工出口區北一路18號

（英文）

國籍：（中文）中華民國 （英文）

代表人：（中文）焦佑衡

（英文）

■ 有創作人或申請人續頁（創作人或申請人欄位不敷使用時，請註記此便用續頁）

562240

創作人 2

姓名：(中文) 劉仲杰

(英文)

住居所地址：(中文) 高雄市前鎮區 806 英明一路 97 之 1 號

(英文)

國籍：(中文) 中華民國 (英文)

創作人 3

姓名：(中文) 洪慧齡

(英文)

住居所地址：(中文) 高雄市鼓山區 804 鼓山二路 202 巷 4 號

(英文)

國籍：(中文) 中華民國 (英文)

562240

肆、中文新型摘要

一種具有打線橋接晶片之電子封裝件，包含一基板、一銲黏於基板上之功能晶片、至少一銲黏於基板上並位於功能晶片之一側邊的打線橋接晶片、一與基板相連結並保護功能晶片與打線橋接晶片之封裝膠體、多數銲線，及多數銲黏於該基板底面上的電性連接件，以該些銲線之一電性連結該功能晶片之一預定電子節墊與該打線橋接晶片之一相對應架橋銲墊，再以另一銲線電性連結該相對應架橋銲墊與基板之一預定與功能晶片之電子節墊電性連接之一電性連接墊，而使該功能晶片處理之電子信號可傳輸至該電路機板，以縮減銲線長度及傾斜角度，以提昇封裝良率。

伍、英文新型摘要

562240

陸、(一)、本案指定代表圖為：第 四 圖

(二)、本代表圖之元件代表符號簡單說明：

2	電子封裝件	231	底面
21	基板	232	銲線面
211	上表面	24	銲線
212	下表面	25	封裝膠體
213	電路佈局	26	電性連接件
214、214'	電性連接墊	3	架橋銲墊
22	功能晶片	31	第一銲點部
221	底面	32	第二銲點部
222	電性連接面		
223	電子節墊		
23	打線橋接晶片		

562240

主張優先權聲明

☐ 本案係符合專利法第二十八條第一項☐第一款但書或☐第二款但書規定之期間，其日期為：_____

☐ 本案已向下列國家（地區）申請專利，申請日期及案號資料如下：

【格式請依：申請國家（地區）；申請日期；申請案號　順序註記】

1._____

2._____

3._____

☐ 主張專利法第一〇五條準用第二十四條第一項優先權：

【格式請依：受理國家（地區）；日期；案號　順序註記】

1._____

2._____

3._____

4._____

5._____

6._____

7._____

8._____

9._____

10._____

☐ 主張專利法第一〇五條準用第二十五條之一第一項優先權：

【格式請依：申請日；申請案號　順序註記】

1._____

2._____

3._____

562240

【新型所屬之技術領域】

本新型是有關於一種電子封裝件，特別是指一種具有多數晶片之電子封裝件。

【先前技術】

由於各項電子產品不斷追求輕、薄、體積小，因此，將多數不同功能的晶片模組式封裝於單一電子封裝件中，使單一電子封裝件具有多數不同的功能，而取代多數僅具有單一功能的電子封裝件，以減少某一電器產品之一電路機板所銲黏的電子封裝件的數目，進而縮減電路機板、乃至於電器產品本身的體積，已為封裝業者所研究發展多年，例如，中華民國專利第 428258 號「具有柵陣列形式之連接端子的半導體裝置」、443582 號「堆疊式晶片尺寸構裝」、484749 號「一種應用於球閘陣列封裝製程之堆疊技術」，及第 498513 號「微機器堆疊線結封裝」等案，以及美國專利公開 US 2002/0153615A1 號「Multi-chip Package Type Semiconductor Device」、US6407456B1「Multi-chip Device Utilizing a Flip Chip and Wire Bond Assembly」.....等案，均各自揭示相關之不同技術特徵。

參閱第一、二圖，一般具有多數功能不同晶片之電子封裝件 1，是包含一基板 11、多數自該基板 11 上依序向上堆疊銲黏之功能晶片 12、12'（本實施例中以二功能晶片為例說明）、多數相對應電性連結基板 11 與功能晶片 12、12'、功能晶片 12 與功能晶片 12'之銲線 13、一連結於基板 11 上並包覆該些功能晶片 12、12'、銲線 13 之封

562240

裝膠體 14，及多數銲點於基板 11 之一底面的電性連接件 15。

熟悉封裝過程之打線製程（wire bond）人士皆知，由於基板 11 與其相鄰靠之功能晶片 12、功能晶片 12 與功能晶片 12'間，及基板 12 與最上層之功能晶片 12'間之高度差異各不相同，因此在以銲線 13 相對應電性連結基板 11 與功能晶片 12、12'時，會因為此等高度差而使得打線製程相對困難，而降低良率，同時，也會因為此等銲線型態，使後續之封膠製程的模流（molding flow）相對複雜而不可控，因而增加封膠製程的困難。

此外，當該二功能晶片 12、12'彼此面積差異極大，及/或該一功能晶片 12'與基板 11 之面積差異極大時，除了會使銲線 13 的長度增加，而使得銲線 13 本身飄移扭曲，易與另一相鄰近之銲線 13 接觸而導致短路外，也會使得銲線 13 與晶片 12、12'之一側邊的夾角過小，而違反客戶所訂定的設計規則（design rule），增加業者成本負擔。

再者，以此種依序向上堆疊功能晶片 12、12'的封裝方式，必然會使得電子封裝件 1 的厚度增加，如需維持標準電子封裝件之規格厚度，勢必必須解決例如如何減少功能晶片 12、12'、基板 11 之厚度，以及降低銲線 13 高度..等等複雜的製程問題。

由上述可知，雖然以堆疊功能晶片 12、12'的方式將多數功能晶片 12、12'封裝於單一電子封裝件 1 中，確實可以縮減電子產品中的電子封裝件的數目，而達到縮減電

562240

子產品體積的目的，然而，此種封裝方式除了會使得電子封裝件 1 厚度增加，而不符合規格的問題之外，在打線製程上更需要研究改進，而提昇銲線可靠度。

【新型內容】

因此，本新型之目的，是在提供一種具有打線橋接晶片之電子封裝件，以縮減銲線長度及控制銲線與晶片夾角，進而提昇銲線可靠度。

於是，本新型一種具有打線橋接晶片之電子封裝件，包含一基板、一銲黏於該基板上之功能晶片、一與該基板相連結之封裝膠體，及多數銲黏於該基板相反於銲黏該功能晶片之一底面上的電性連接件。

該基板具有預定電路佈局及多數分別與該電路佈局相電性連結之電性連接墊；該功能晶片可處理電子信號，並具有多數分別與該基板之電性連接墊預定相對應電性連結之電子節墊；該封裝膠體包覆該基板之電路佈局、多數電性連接墊與該功能晶片而與外界相隔絕；該些電性連接件與該基板之電路佈局相電性連結，並可電性連結至一電路機板上。

該電子封裝件之特徵在於更包含至少一銲黏於該基板上之打線橋接晶片，及多數銲線，該打線橋接晶片包括多數彼此不相電性導通之架橋銲墊，該每一架橋銲墊具有二相對遠離並相互電性導通之第一銲黏部與第二銲黏部，且該第一銲黏部是相對靠近該功能晶片之一預定電子節墊，該第二銲黏部是相對靠近該功能晶片之預定電子節墊預定

562240

電性連接之該基板的電性連接墊，同時，以該等銲線其中之一電性連結該功能晶片之預定電子節墊與該架橋銲墊之第一銲黏部，以另一銲線電性連結該第二銲黏部與該基板之預定電性連接墊，而使該功能晶片處理之電子信號可傳輸至該電路機板。

【實施方式】

本新型之前述以及其他技術內容、特點與功效，在以下配合參考圖式之一(數)較佳實施例的詳細說明中，將可清楚的明白，另外，在本新型被詳細描述之前，要注意的是，在以下的說明中，類似的元件是以相同的編號來表示。

同時參閱第三、四圖，本新型具有打線橋接晶片之電子封裝件 2 的一第一較佳實施例，是包含一基板 21、一銲黏於該基板 21 上之功能晶片 22、一銲黏於該基板 21 上之打線橋接晶片 23、多數銲線 24、一與該基板 21 相連結之封裝膠體 25、及多數電性連接件 26。

該基板 21 呈一矩形，具有一上表面 211、一相反於該上表面 211 之下表面 212、預定態樣之電路佈局 213，及多數電性連接墊 214、214'，該電路佈局 213 是依照該功能晶片 22 之預定電子功能不同而有不同設計態樣，因此部分與本新型創作重點無關，故不多加贅述；該些電性連接墊 214、214'分別布設於該上、下表面 211、212 之一外周部，並分別與電路佈局 213 相電性連結。

該功能晶片 22 可計算、傳輸、接受電子信號，具有一與該基板 21 之上表面 211 相連結之底面 221、一相反

562240

於該底面 221 之電性連接面 222，及多數布設於該電性連接面 222 上的電子節墊 223，該些電子節墊 223 分別預定相對應地以多數銲線 24 與該基板 21 之上表面 211 布設之電性連接墊 214 電性連結。

該打線橋接晶片 23 不具有任何電子運算功能（function），但其製程與功能晶片 22 相同，是應用半導體製程以矽、及/或包含矽之化合物為材料製成，並使其厚度相對應於該功能晶片 22 之厚度，具有一與該基板 21 之上表面 211 相連結之底面 231、一相反於該底面 231 之一銲線面 232，及多數彼此不相電性導通之架橋銲墊 3。

該每一架橋銲墊 3 是以導電材料，例如金、鎳、銅、鋁、或是至少其中含有金、鎳、銅、鋁等成分之合金製成，以預定態樣設佈於該打線橋接晶片 23 之銲線面 232 上，此等材料之選擇，需視選用銲線之材質，使得銲線 24 與架橋銲墊 3 能夠相同或近似材料之結合，以取得最大鍵結力。

該每一架橋銲墊 3 具有二相對遠離並相互電性導通之第一銲黏部 31 與第二銲黏部 32，且該第一銲黏部 31 是相對靠近該功能晶片 22 之一預定電子節墊 223，該第二銲黏部 32 是相對靠近該功能晶片 22 之預定電子節墊 223 預定電性連接之基板 21 的電性連接墊 214，在本實施例中，該些架橋銲墊 3 是分別以成 L 形及矩形態樣，依序以該些第一銲黏部 31 較集中，且該些第二銲黏部 32 較疏鬆之放射狀分布，使該等第一銲黏部 31 更加相對靠近該功

562240

能晶片 22 之電子節墊 223，且第二銲黏部 32 更加相對靠近該基板 21 的電性連接墊 214；在此要特別說明的是，由於適用不同電子產品的功能晶片之電子節墊與基板之電性連接墊的分布方式均有所差異，故打線橋接晶片，不但其本身形狀必須配合不同功能晶片與基板，同時打線橋接晶片之多數架橋銲墊，其形狀及分布方式，亦必須配合功能晶片之電子節墊與基板之電性連接墊的分布方式而有所不同，由於此種形狀圖案種類變化繁多，在此不一一舉例說明。

熟悉封裝技術人士皆知，若就功能晶片 22 之單一預定電子節墊 223 而言，原本僅需以一根銲線 24 電性連結之功能晶片 22 的一預定電子節墊 223 與該基板 21 之一預定電性連接墊 214，即可達成電性連接功能晶片 22 與基板 21 之目的；但在本新型中，相鄰近該打線橋接晶片 23 之多數電子節墊 223 是分別以該等銲線 24 其中之一先電性連結該功能晶片 22 之預定電子節墊 223 與該架橋銲墊 3 之第一銲黏部 31，再以另一銲線 24 電性連結該第二銲黏部 32 與該基板 21 之預定電性連接墊 214，其他側邊則依照一般打線方式，直接以銲線 24 電性連接功能晶片 22 的電子節墊 223 與基板 21 之電性連接墊 214，藉此，可以縮短並同時降低原本銲線 24 長度及高度，提昇打線製程之良率，如此依序將功能晶片 22 之電子節墊 223 以該些銲線 24 電性連結該基板 21 之多數電性連接墊 214，而使該功能晶片 22 處理運算之電子信號可傳輸至該基板

562240

捌、新型說明(二)

21。

該封裝膠體 25 為一高分子聚合物，連結於該基板 21 之上表面 211，並包覆基板 21 之電路佈局 213 與上表面 211 之多數電性連接墊 214、功能晶片 22、打線橋接晶片 23，及多數銲線 24，使其與外界相隔絕，而不致氧化腐蝕。

該些電性連接件 26 分別相對應地銲黏於該基板 21 下表面 212 之多數電性連接墊 214'上，而與該基板 21 之電路佈局 213 相電性連接，而可使該電子封裝件 2 電性連結至一預定電子產品之一電路載板上（圖未示出），使該功能晶片 22 處理運算之電子信號可傳輸至該基板 21 後，再傳輸至該電路基板而發揮該電子封裝件 2 之預定功能。

由上述可知，本新型以不具有任何電子運算功能之打線架橋晶片 23，銲黏於功能晶片 22 之一側邊，藉由多數彼此不相電性導通之架橋銲墊 3，使原本預定電性連結之功能晶片 22 的電子節墊 223 與基板 21 的電性連接墊 214，分別以二銲線 24 先電性連結功能晶片 22 之電子節墊 223 與架橋銲墊 3，再以另一銲線 224 電性連結該架橋銲墊 3 與該基板 21 之電性連接墊 214，藉此，可以大幅縮減單一銲線 24 之長度與銲線高度；熟悉半導體製程與封裝技術製程人士均知，雖然，增加一打線橋接晶片 23 會增加部分材料成本，然而合併考量後，由於可以縮短並同時降低原本銲線 24 長度及高度，使銲線 24 之可控程度相對提昇許多，因而提昇打線製程之良率，同時，較短與較

562240

低的銲線 24，亦較不受後續封膠製程的模流的影響，而可相對提昇封裝製程的良率，因而可以總擴地降低整個生產成本，而符合業者需求。

上述本新型之說明，是適用功能晶片 22 與基板 21 之面積差異在預定範圍內，而可以改變銲黏功能晶片 22 與基板 21 之相對位置，再以一打線橋接晶片 23 輔助後，即可使所有銲線 24 的高度、長度，及其與功能晶片 22 之一側邊的相對夾角等等銲線參數，均滿足客戶要求之設計規則之狀況。

當功能晶片 22 與基板 21 之面積差異極大，而無法以改變銲黏功能晶片 22 與基板 21 之相對位置，再以單一打線橋接晶片 23 輔助後，即可使所有銲線 24 的高度、長度，及其與功能晶片 22 之一側邊的相對夾角等等銲線參數，均滿足客戶要求之設計規則時，則可以如第五圖所示，本新型具有打線橋接晶片之電子封裝件 2'的一第二較佳實施例所示，以多數不同打線橋接晶片 23、23'分設於功能晶片 22 之不同側邊，本實施例以二打線橋接晶片 23、23'分設於功能晶片 22 之相鄰二側邊為例說明，藉以縮短並同時降低原本銲線 24 長度及高度，因其細部構造均已於該第一較佳實施例充分說明，故在此不再多加贅述。

參閱第六圖，本新型具有打線橋接晶片之電子封裝件的一第三較佳實施例，是與上述二例相似，其不同處僅在於，由於不同之功能晶片 22 在設計時，常會因電路需要，而必須以功能晶片 22 之單一電子節點 223 銲黏多數條

銲線 24 至基板 21 的多數相對應電性連接墊 214 上，或是功能晶片 22 之多數電子節墊 223 銲黏多數條銲線 24 至基板 21 的單一相對應電性連接墊 214 上，因此，本實施例電子封裝件 2"之每一架橋銲墊 3 之第一銲黏部 31 與第二銲黏部 32，均可選擇地供至少一條銲線 24 的一端部相銲黏，由於架橋銲墊 3 之材質與銲線 24 之材質相同或近似，因此，該第一、二銲黏部 31、32 即使銲固多數根銲線 24 亦不會影響每根銲線 24 之連接處的牢固度，而可適合不同功能晶片 22 之電性連接需求。

此外，本新型具有打線橋接晶片之電子封裝件，亦可應用於昔知堆疊多數功能晶片之電子封裝件中，在打線封裝晶片 23 及功能晶片 22 與該基板 21 之間，再多加設一層或多層功能晶片而已，由於此等結構僅為簡單推知運用且種類繁多，不再一一多加舉例說明。

歸納上述，本新型具有打線橋接晶片之電子封裝件 2、2'，藉由增加不具有任何電子運算功能之打線架橋晶片 23、23'，不但可大幅縮減單一銲線 24 之長度與銲線 24 高度，提昇打線可控度，並可減少後續封膠製程模流對銲線之影響，而相對提昇封裝製程的良率，因而降低整個生產成本，符合業者需求，確實能達到本新型之目的。

惟以上所述者，僅為本新型之較佳實施例而已，當不能以此限定本新型實施之範圍，即大凡依本新型申請專利範圍及新型說明書內容所作之簡單的等效變化與修飾，皆應仍屬本新型專利涵蓋之範圍內。

562240

捌、新型說明（10）

【圖式簡單說明】

第一圖是一剖視圖，說明昔知具有複數層相互堆疊之晶片的球格陣列封裝件之結構；

第二圖是第一圖之一正面上視圖，說明該些複數層相互堆疊之晶片以銲線相互電性連結之態樣；

第三圖是一剖視圖，說明本新型具有打線橋接晶片之電子封裝件的一第一較佳實施例之結構；

第四圖是第三圖之一正面上視圖，說明一功能晶片、一打線橋接晶片，及一基板以銲線相互電性連結之態樣；

第五圖是本新型具有打線橋接晶片之電子封裝件的一第二較佳實施例之一正面上視圖，並說明一功能晶片藉由二打線橋接晶片而與基板相互以銲線電性連結，以縮短銲線之長度與分布角度之態樣；及

第六圖是本新型具有打線橋接晶片之電子封裝件的一第三較佳實施例之一正面上視圖，並說明一打線橋接晶片之架橋銲墊的第一銲黏部與第二銲黏部，分別可選擇地供至少一條銲線的二端部相銲黏。

562240

圖式說明(一)

【圖式之主要元件代表符號簡單說明】

1	電子封裝件	222	電性連接面
11	基板	223	電子節墊
12、12'	功能晶片	23、23'	打線橋接晶片
13	銲線	231	底面
14	封裝膠體	232	銲線面
15	電性連接件	24	銲線
2、2'、2"	電子封裝件	25	封裝膠體
21	基板	26	電性連接件
211	上表面	3	架橋銲墊
212	下表面	31	第一銲點部
213	電路佈局	32	第二銲點部
214、214'	電性連接墊		
22	功能晶片		
221	底面		

562240

拾、申請專利範圍

1. 一種具有打線橋接晶片之電子封裝件，該電子封裝件包含一基板、一銲黏於該基板上之功能晶片、一與該基板相連結之封裝膠體，及多數銲黏於該基板相反於銲黏該功能晶片之一底面上的電性連接件，該基板具有預定電路佈局及多數分別與該電路佈局相電性連結之電性連接墊，該功能晶片可處理電子信號，並具有多數分別與該基板之電性連接墊預定相對應電性連結之電子節墊，該封裝膠體包覆該基板之電路佈局、多數電性連接墊與該功能晶片而與外界相隔絕，該些電性連接件與該基板之電路佈局相電性連結，並可電性連結至一電路機板上；其特徵在於：

該電子封裝件更包含至少一銲黏於該基板上之打線橋接晶片，及多數銲線，該打線橋接晶片包括多數彼此不相電性導通之架橋銲墊，該每一架橋銲墊具有二相對遠離並相互電性導通之第一銲黏部與第二銲黏部，且該第一銲黏部是相對靠近該功能晶片之一預定電子節墊，該第二銲黏部是相對靠近該功能晶片之預定電子節墊預定電性連接之該基板的電性連接墊，同時，以該等銲線其中之一電性連結該功能晶片之預定電子節墊與該架橋銲墊之第一銲黏部，以另一銲線電性連結該第二銲黏部與該基板之預定電性連接墊，而使該功能晶片處理之電子信號可傳輸至該電路機板。

2. 依據申請專利範圍第 1 項所述之具有打線橋接晶片之電子封裝件，其中，該打線橋接晶片之厚度是相對應於該功能

562240

晶片之厚度。

3. 依據申請專利範圍第1項所述之具有打線橋接晶片之電子封裝件，其中，該打線橋接晶片是以矽，及/或包含矽之化合物為材料。

4. 依據申請專利範圍第1項所述之具有打線橋接晶片之電子封裝件，其中，該打線橋接晶片之架橋銲墊是以導電材料製成。

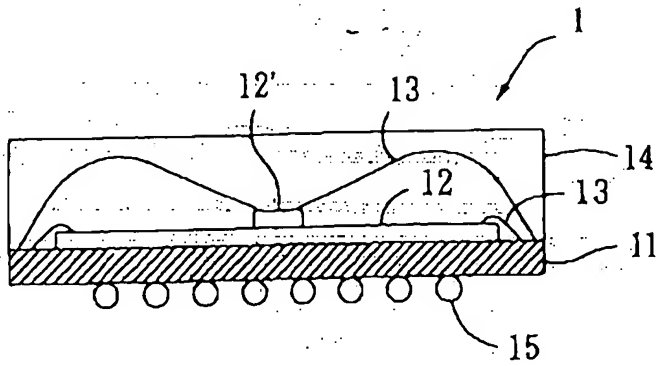
5. 依據申請專利範圍第4項所述之具有打線橋接晶片之電子封裝件，其中，該打線橋接晶片之架橋銲墊是以金、鎳、銅、鋁、至少含金之合金、至少含鎳之合金、至少含銅之合金，及/或至少含鋁之合金製成。

6. 依據申請專利範圍第1項所述之具有打線橋接晶片之電子封裝件，其中，該打線橋接晶片之架橋銲墊是以預定態樣鍍佈於該打線橋接晶片之一表面。

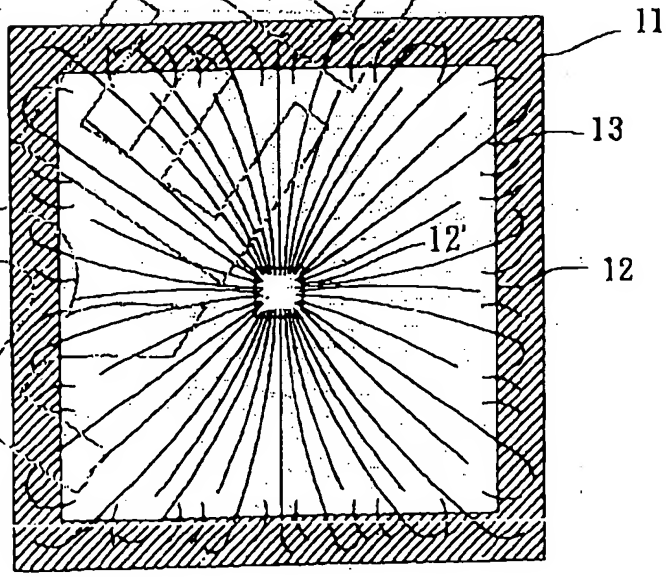
7. 依據申請專利範圍第1項所述之具有打線橋接晶片之電子封裝件，其中，該每一架橋銲墊之第一銲黏部與第二銲黏部，是分別可選擇地供至少一條銲線的一端部相銲黏。

562240

拾、圖式



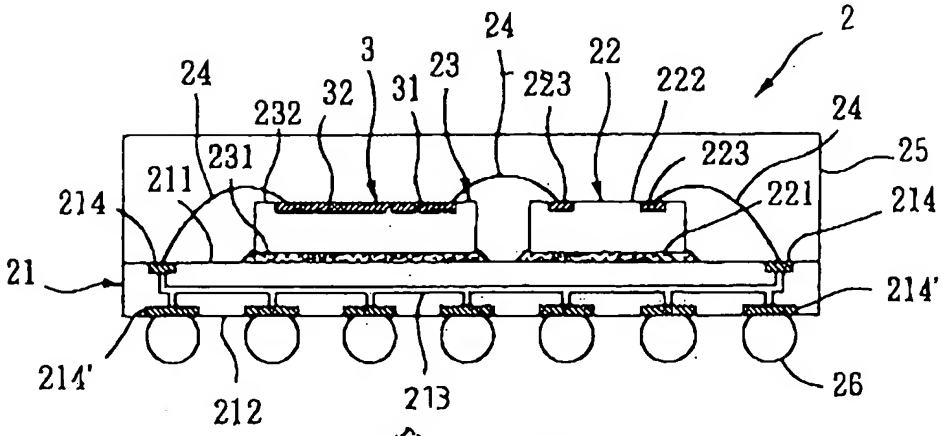
第一圖



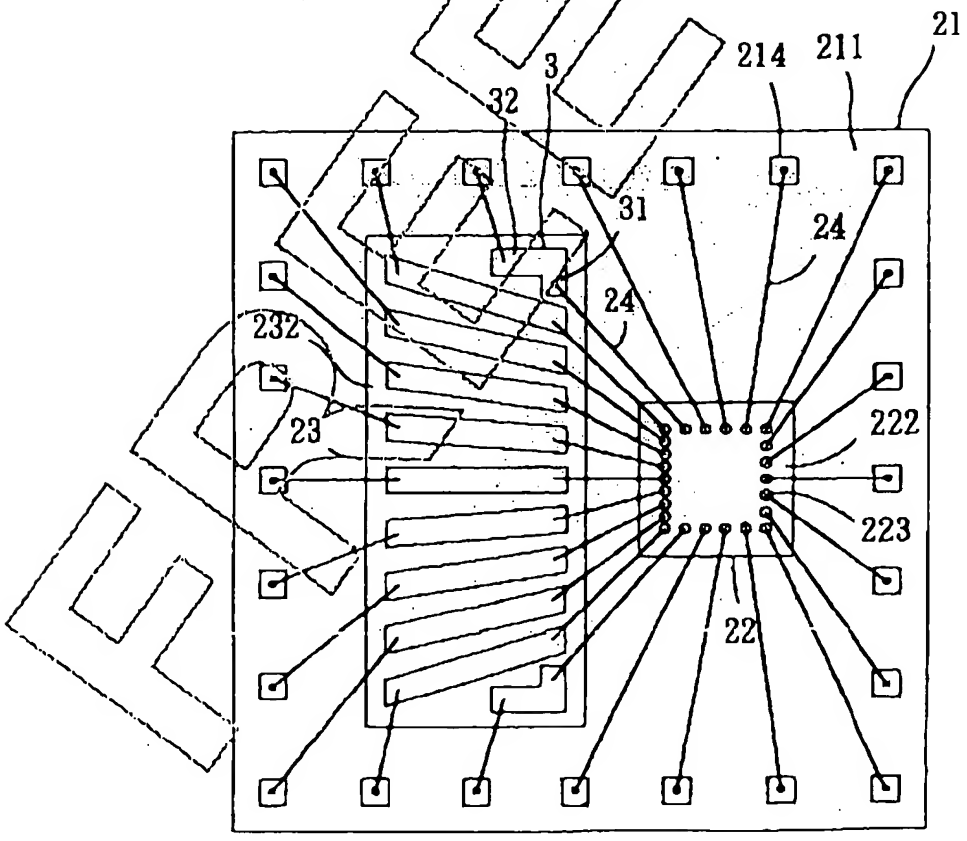
第二圖

562240

拾、圖式



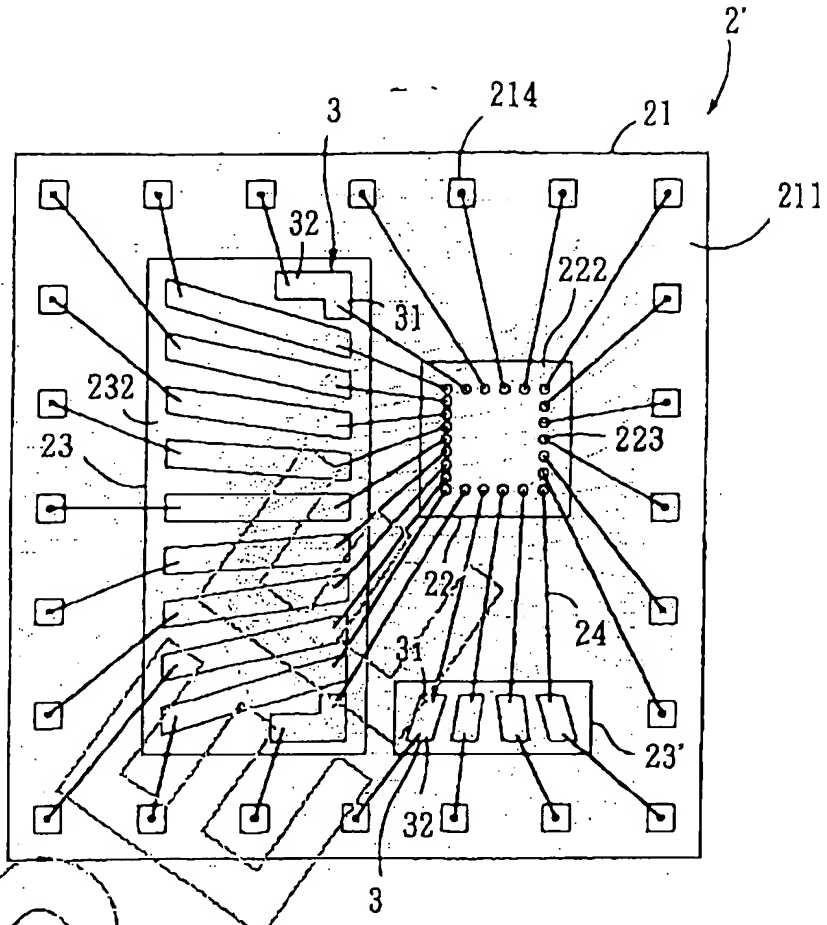
第三圖



第四圖

562240

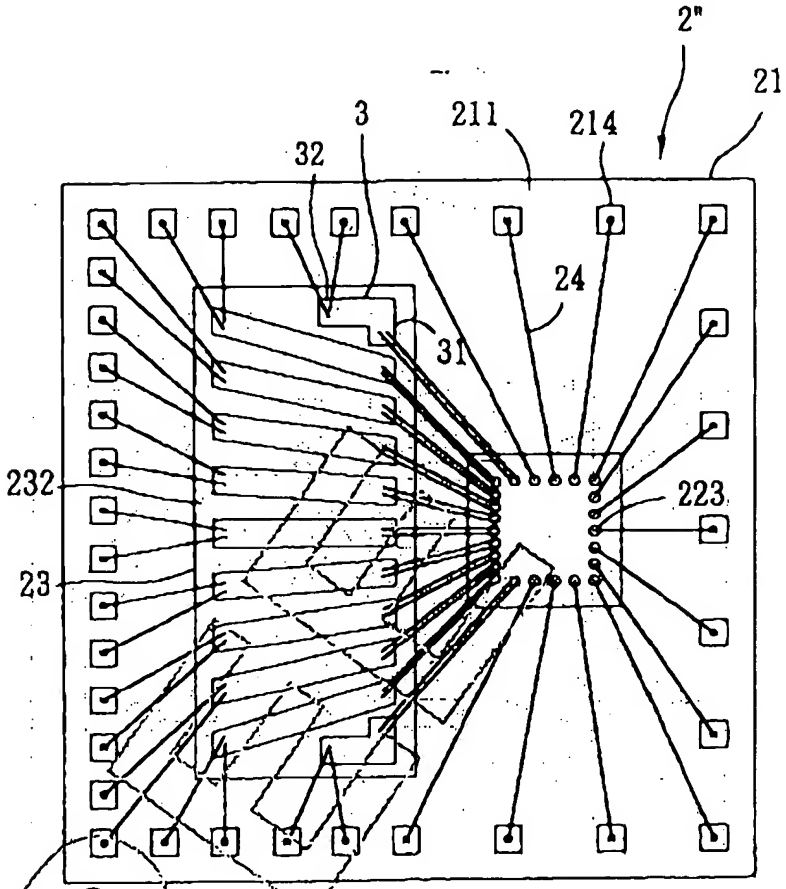
拾、圖式



第 五 圖

562240

拾、圖式



第 六 圖